

Q.3

	<u>Allocation</u>				<u>Max</u>				<u>Available</u>			
	A	B	C	D	A	B	C	D	A	B	C	D
T ₀	0	0	1	2	0	0	1	2	1	5	2	0
T ₁	1	0	0	0	1	7	5	0				
T ₂	1	3	5	4	2	3	5	6				
T ₃	0	6	3	2	0	6	5	2				
T ₄	0	0	1	4	0	6	5	6				

a.) What is the content of the matrix Need?
Need Matrix (Max - Allocation)

	A	B	C	D
T ₀	0	0	0	0
T ₁	0	7	5	0
T ₂	1	0	0	2
T ₃	0	0	2	0
T ₄	0	6	4	2

$\langle T_0, T_2, T_3, T_4, T_1 \rangle$

b) Is the system in a safe state? $\rightarrow$ Yes

① Need [T₀] ≤ Available then,

$$\text{Ava} = [0 \ 0 \ 1 \ 2] + [1 \ 5 \ 2 \ 0]$$

$$= 1 \ 5 \ 3 \ 2$$

Finish [T₀] = true.

② Need [T₁] ≤ Ava [0 7 5 0] ≤ 1 5 3 2 X

③ Need [T₂] ≤ Ava [1 0 0 2] ≤ 1 5 3 2 ✓

$$\text{Ava} = \begin{matrix} 1 & 3 & 5 & 4 \\ 1 & 0 & 0 & 2 \end{matrix} + 1 \ 5 \ 3 \ 2 = \begin{matrix} 2 & 8 & 8 & 6 \\ 2 & 5 & 3 & 4 \end{matrix}$$

Finish [T₂] = True

④ Need $[T_3] \leq \text{Ava} \Rightarrow 0020 \leq 2886$

$$\begin{array}{r} \text{Ava} = \begin{array}{r} 2 \ 8 \ 8 \ 6 \\ 0 \ 6 \ 3 \ 2 \\ \hline 2 \ 14 \ 11 \ 8 \end{array} \end{array}$$

$$\text{Ava} [2 \ 14 \ 11 \ 8]$$

⑤ Need $[T_4] \leq \text{Ava} \Rightarrow 0642 \leq 214118$

$$\begin{array}{r} \begin{array}{r} 2 \ 14 \ 11 \ 8 \\ 0 \ 0 \ 1 \ 4 \\ \hline 2 \ 14 \ 12 \ 12 \end{array} \end{array}$$

$$\text{Ava} = [2 \ 14 \ 12 \ 12]$$

⑥ Need $[T_1] \leq \text{Ava} \Rightarrow [0750] \leq [2141212]$

$$\begin{array}{r} \begin{array}{r} 2 \ 14 \ 12 \ 12 \\ 1 \ 0 \ 0 \ 0 \\ \hline 3 \ 14 \ 12 \ 12 \end{array} \end{array}$$

⑦ If a request from Thread T_1 arrives for $(0, 4, 2, 0)$ can the request be granted immediately?

Ans: Yes, $(0, 4, 2, 0) \leq (1, 5, 2, 0)$
Request Available

8.9

	Allocation	Need	Max	Avail
	A B C D	A B C D	A B C D	
T ₀	3 0 1 4	2 1 0 3	5 1 1 7	0 3 0 1
T ₁	2 2 1 0	1 0 0 1	3 2 1 1	
T ₂	3 1 2 1	0 2 0 0	3 3 2 1	
T ₃	0 5 1 0	4 1 0 2	4 6 1 2	
T ₄	4 2 1 2	2 1 1 3	6 3 2 5	

finish [T₀] = false

finish [T₁] = false

finish [T₄] = false

< T₂, T₁, T₃,

Need	Available	Checking
2 1 0 3	0 3 0 1	Need ≤ Avail X
1 0 0 1	0 3 0 1	Need ≤ Avail X
0 2 0 0	0 3 0 1 3 1 2 1 3 4 2 2	Need ≤ Avail ✓ Finish [T ₂] = True
4 1 0 2	3 4 2 2	Need ≤ Avail X
2 1 1 3	3 4 2 2	Need ≤ Avail X
2 1 0 3	3 4 2 2	Need ≤ Avail X
1 0 0 1	3 4 2 2 2 2 1 0 5 6 3 2	✓ Finish [T ₁] = True
4 1 0 2	5 6 3 2 0 5 1 0 5 11 4 2	✓ Finish [T ₃] = True
2 1 1 3	5 11 4 2	X
2 1 0 3	5 11 4 2	X

Not a safe sequence
So, system enters into dead
locks.

(3)

	<u>Allocation</u>	<u>Max</u> <u>need</u>	<u>Max</u> <u>need</u>	<u>Available</u>
T ₀	3 1 4 1	6 4 7 3	3 3 3 2	2 2 2 4
T ₁	2 1 0 2	4 2 3 2	2 1 3 0	
T ₂	2 4 1 3	2 5 3 3	0 1 2 0	
T ₃	4 1 1 0	6 3 3 2	2 2 2 2	
T ₄	2 2 2 1	5 6 7 5	3 4 5 4	

<u>Need</u>	<u>Available</u>	<u>checking</u>	
3 3 3 2	2 2 2 4	need ≤ Avail	< T ₂ , T ₃ , T ₄ , T ₀ , T ₁ >
2 1 3 0	2 2 2 4	need ≤ Avail	
0 1 2 0	2 2 2 4 + 2 4 1 3	need ≤ Avail ✓ finish [T ₂] = True	
2 2 2 2	4 6 3 7 4 1 1 0	need ≤ Avail ✓ finish [T ₃] = True	
3 4 5 4	8 7 4 7 2 2 2 1	need ≤ Avail ✓ finish [T ₄] = True	
3 3 3 2	10 9 6 8 3 1 4 1	need ≤ Avail ✓ finish [T ₀] = True	
2 1 3 0	13 10 10 9 2 1 0 2 15 11 10 11	need ≤ Avail finish [T ₁] = True	

The system is in safe state & the
safe sequence is < T₂, T₃, T₄, T₀, T₁ >

P₃ :- Need 7 3 3 Variable

10	4	7
0	2	0
10	6	7

Finish[P₃] = true & Variable =

<P₁ P₄ P₀ P₂ P₃> Safe Sequence

Time Complexity :- $n \times \left(\frac{n}{m}\right)$

↓ ↓

No. of Iterations for each Iteration

	Allocation	Max	Need	Available
		7 5 3	7 4 3	3 3 2
T ₀	0 1 0			
T ₁	2 0 0	3 2 2	1 2 2	
T ₂	3 0 2	9 0 2	6 0 0	
T ₃	2 1 1	2 2 2	0 1 1	
T ₄	0 0 2	4 3 3	4 3 1	

Step-1:- finish[T₀] = false.

Available
Work = 3 3 2

finish[T₄] = false.

Step-2:-

finish[T₀] = false && ~~[0 1 0]~~ [7 4 3] ≤ 3 3 2 X

T₁ = false && [1 2 2] ≤ 3 3 2 ✓

So allocate to T₁

Step-3:- T₁ finish[T₁] = true;

Work = 3 3 2 + 2 0 0

W = 5 3 2

<T₁, T₃>

T₂ = false && 6 0 0 ≤ 5 3 2 X

T₃ = false && 0 1 1 ≤ 5 3 2 ✓

finish(T₃) = True

W = $\begin{array}{r} 5\ 3\ 2 \\ 2\ 1\ 1 \\ \hline 7\ 4\ 3 \end{array}$

W = 7 4 3

$$T_4 = \text{false} \text{ \&\& } 4 \ 3 \ 1 \leq 7 \ 4 \ 3$$

$$\text{so, } T_4 = \text{True}$$

$$\text{Work} = \begin{array}{r} 7 \ 4 \ 3 \\ 0 \ 0 \ 2 \\ \hline 7 \ 4 \ 5 \end{array}$$

After 1st Iteration,

$$T_1, T_3, T_4 = \text{true} \quad T_0, T_2 = \text{false}$$

$$T_0 = \text{false} \text{ \&\& } 7 \ 4 \ 3 \leq 7 \ 4 \ 5 \checkmark$$

$$\text{so, } T_0 = \text{true}$$

$$W = \begin{array}{r} 7 \ 4 \ 5 \\ + 0 \ 1 \ 0 \\ \hline 7 \ 5 \ 5 \end{array}$$

$$T_2 = \text{false} \text{ \&\& } 7 \ 6 \ 0 \ 0 \leq 7 \ 5 \ 5 \checkmark$$

$$\text{so, } T_2 = \text{true}$$

$$W = \begin{array}{r} 7 \ 5 \ 5 \\ + 3 \ 0 \ 2 \\ \hline 10 \ 5 \ 7 \end{array}$$

After 2nd Iteration all the resources are become true
safety

so, list is)

$$\langle T_1, T_3, T_4, T_0, T_2 \rangle$$

Safety
sequence

Request - R

Resource - Request Algorithm

Steps:-

① If $Request_i \leq Need_i$, go to step 2. Otherwise raise an error condition, since the thread has exceeded its maximum claim.

② If $Request_i \leq Available$, go to step 3. Otherwise T_i must wait, since the resources are not available.

③ Have the system pretend to have allocated the requested resources to thread T_i by modifying the state as follows:-

$$\begin{aligned} Available &= Available + Request_i \\ Allocation &= Allocation_i + Request_i \\ Need &= Need - Request_i \end{aligned}$$

Ex:-

	<u>Allocation</u>	<u>Request</u>	<u>Available</u>
T_0	0 1 0	0 0 0	0 0 0
T_1	2 0 0	2 0 2	
T_2	3 0 3	0 0 0	
T_3	2 1 1	1 0 0	
T_4	0 0 2	0 0 2	

→ firstly take a process which has request as 0 0 0
so, firstly take T_2 then,

$$Avail = 0 0 0 + 3 0 3 = 3 0 3$$

then we go to T_4 where $0 0 2 \leq 3 0 3$
 $\{ 3 0 3 \} \rightarrow 3 0 5$

$$T_0 \Rightarrow \quad \cancel{0} \quad 0 \quad 0 \quad 0 \leq 305$$

$$\begin{array}{r} \text{Ava} = \quad 3 \quad 0 \quad 5 \\ \quad \quad 0 \quad 1 \quad 0 \\ \hline \quad \quad 3 \quad 1 \quad 5 \end{array}$$

$$T_1 \Rightarrow \quad 202 \leq 315 \checkmark$$

$$\begin{array}{r} \text{Ava} = \quad 3 \quad 1 \quad 5 \\ \quad \quad 2 \quad 0 \quad 0 \\ \hline \quad \quad 5 \quad 1 \quad 5 \end{array}$$

$$T_3 \Rightarrow \quad 10 \quad 0 \quad \cancel{0} \leq 515$$

$$\begin{array}{r} \text{Ava} = \quad \cancel{0} \quad \cancel{0} \quad \cancel{2} \quad \quad 1 \quad 0 \quad 0 \\ \quad \quad \cancel{5} \quad \cancel{1} \quad \cancel{5} \quad \quad 5 \quad 1 \quad 5 \\ \hline \quad \quad \cancel{5} \quad \cancel{1} \quad \cancel{7} \quad \quad 6 \quad 1 \quad 5 \end{array}$$

$$\langle T_2, T_4, T_0, T_1, T_3 \rangle$$

(a)

$$\langle T_0, T_2, T_3, T_4, T_1 \rangle$$

Recovery from Deadlocks

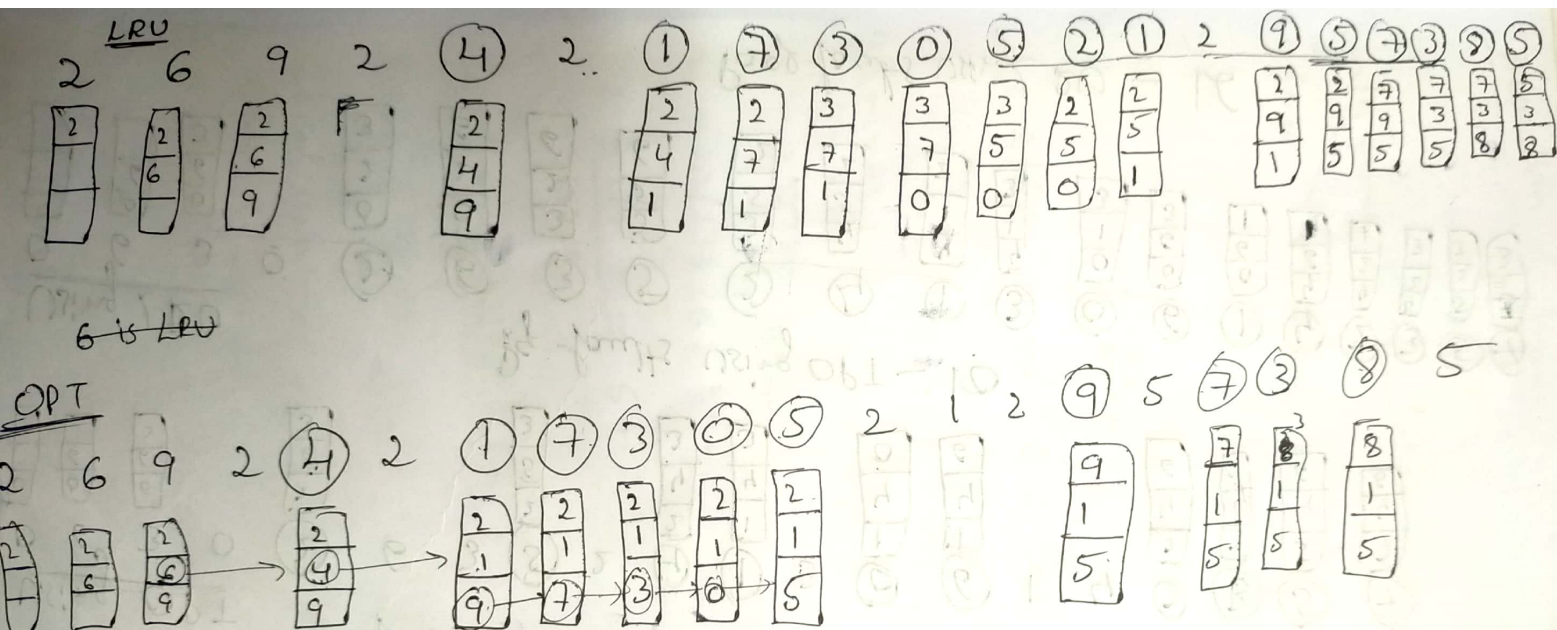
* Process & Thread Termination

→ (i) Abort all deadlocked processes. [Delete whole cycles]

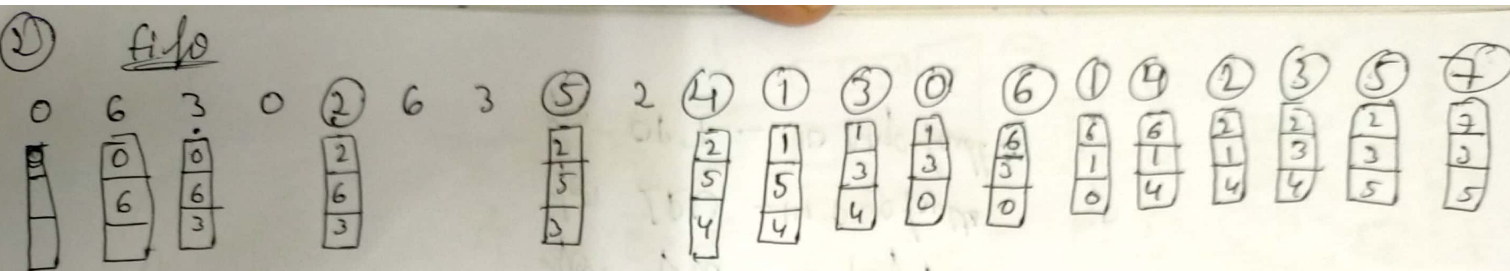
FIFO, LRU, OPT Replacement Algorithms

① - Reference string Using FIFO

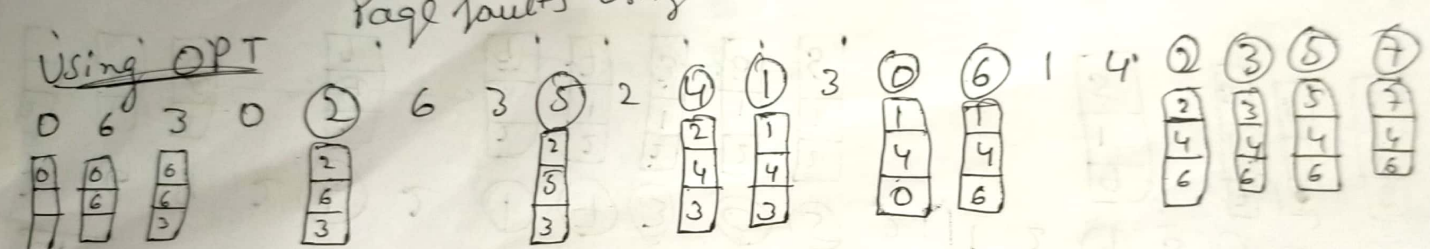
2	6	9	2	1	2	1	7	3	0	5	2	1	2	9	5	7	3	8	5
2	2	2	2	4	4	4	7	7	7	5	5	5	5	9	9	9	3	3	3
	6	6		6	2	2	3	3	3	2	2	2	2	2	5	5	5	8	8
		9		9	9	1	1	1	0	0	0	1	1	1	1	7	7	7	5



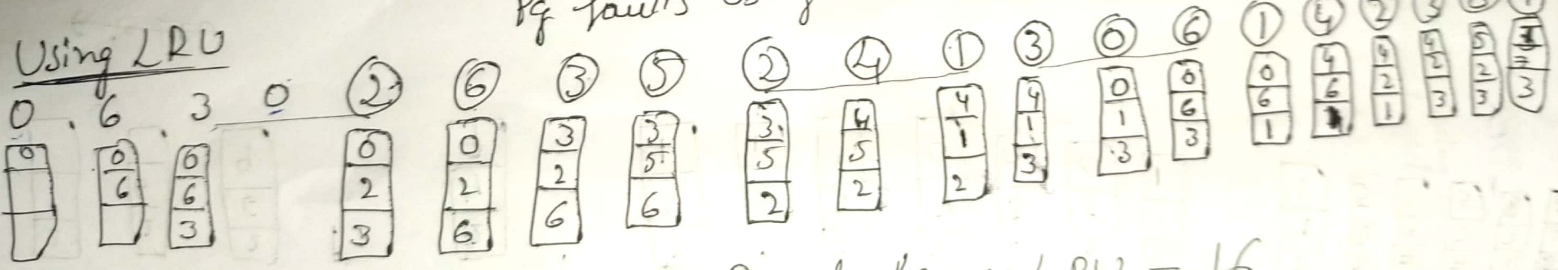
for lru - 15 page faults
 for LRU - 14 page faults
 for OPT - 10 page faults



Page faults using FIFO - 13

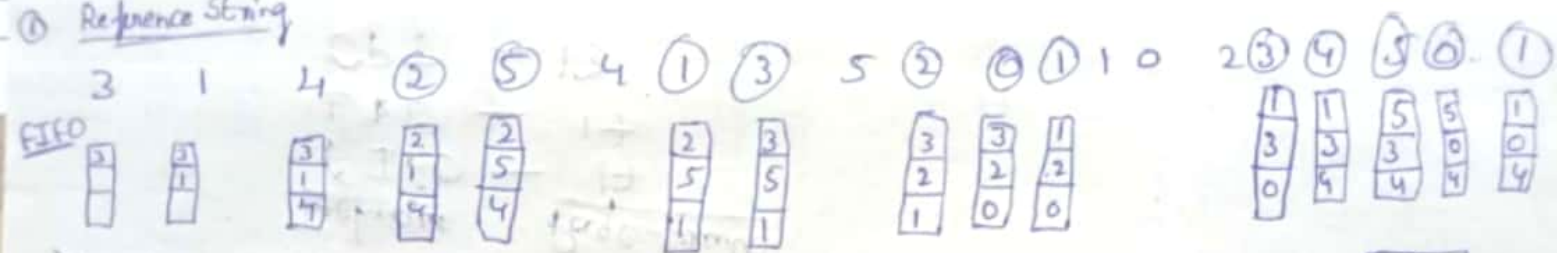


Pg faults using OPT - 10



Page faults using LRU - 16

① Reference String



Page faults using FIFO = 12



Page faults using LRU = 13

