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| **P.V.P Siddhartha Institute of Technology** | | | | | | | | | |
| **Department of Computer Science and Engineering** | | | | | | | | | |
| **Course: B.Tech** | | **Year: II** | **Semester: I** | **Descriptive: II** | **A.Y:2024-25** | | | | |
| **Subject Code: 23ES1304** | | **Subject Name: Digital Logic & Computer Organization** | | | **Regulation:PVP23** | | | | |
| **Duration:1 hr 30 min** | | **Maximum Marks:30 Marks** | | | **Date:27-11-24** | | | **Session: F.N** | |
| **Answer ONE Question from each section. Each Question carries 10 Marks. 3×10M=30M** | | | | | | | | | |
| **Q. No** | **Question** | | | | | **Marks** | **CO** | | **Level** |
| **1 a)** | Explain different types of Instruction Formats with an example for each. | | | | | **5** | CO2 | | L2 |
| **1 b)** | Explain booth multiplication algorithm for the example  (-9 X -13) | | | | | **5** | CO2 | | L3 |
|  | **OR** | | | | |  |  | |  |
| **2 a)** | Differentiate register stack with memory stack. | | | | | **5** | CO2 | | L4 |
| **2 b)** | Discuss in detail various addressing modes. | | | | | **5** | CO2 | | L2 |
|  | | | | | | | | | |
| **3** | Explain Associative memory in detail | | | | | **10** | CO1 | | L2 |
|  | **OR** | | | | |  |  | |  |
| **4 a)** | Discuss about auxiliary memory. | | | | | **5** | CO1 | | L2 |
| **4 b)** | What is cache memory? Explain its operation. | | | | | **5** | CO1 | | L2 |
|  | | | | | | | | | |
| **5 a)** | Explain the purpose I/O interfaces between internal storage and external I/O devices with a neat sketch. | | | | | **5** | CO2 | | L2 |
| **5 b)** | Differentiate strobe control and handshaking mechanisms. | | | | | **5** | CO2 | | L4 |
|  | **OR** | | | | |  |  | |  |
| **6** | With a neat sketch explain the operation of DMA controller and DMA transfer. | | | | | **10** | CO2 | | L2 |

Course Coordinator

Module Coordinator Program Coordinator