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| **P.V.P SIDDHARTHA INSTITUTE OF TECHNOLOGY** | | | |
| **BRANCH : CSE /IT** | | | **REGULATION : PVP23** |
| **Course: B.Tech** | **SUBJECT : DIGITAL LOGIC & COMPUTER ORGANIZATION** | | |
| **Subject Code:23ES1304** | | **Year and Semester: II Year / I Sem** | |
| **QUESTION BANK** | | | |

**UNIT I**

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| **Q.**  **NO** | **PART A** | **CO** | **LEVEL** |
| 1 | Perform 2’s complement on 11001100110. | CO 1 | L1 |
| 2 | Convert the Hexadecimal Number 68BE to binary and octal | CO 1 | L1 |
| 3 | Draw symbol and construct the truth table for NAND, NOR gate. | CO 1 | L1 |
| 4 | Perform (15)10-(28)10 using 10’s Complement. | CO 1 | L1 |
| 5 | Find the output of the given Logic Circuit.  https://sandbox.mc.edu/~bennet/cs110/boolalg/gate4.gif | CO 1 | L2 |
| 6 | What are universal Gates? Why they are called universal gates. | CO 1 | L1 |
| 7 | Convert the following octal to Hexadecimal numbers  i) 2035 ii)1762.46 | CO 1 | L1 |
| 8 | Using 2’s complement perform the following  1101010-110100 | CO 1 | L1 |
| 9 | Simplify the following logic expressions  (A+B)(A’+C)(B+C’) | CO 3 | L2 |
| 10 | Find the Excess 3 code for the following decimal numbers.  i. (1111)10  ii. (0011)10 | CO 1 | L1 |
|  | **PART B** |  |  |
| 11(A) | Convert the following base conversions using Number System.   1. (365.24)10 to ( ? )2 2. (333.45)8 to (?)2 3. (A B 7.D)16 to(?)8 | CO 1 | L2 |
| 11(B) | Convert the (1110001.10001)2 binary number to decimal, hexadecimal and octal numbers | CO 1 | L2 |
| 12(A) | Convert the following octal numbers to hexadecimal i) 2035 ii) 1762.46 iii) 6054.263 | CO 1 | L2 |
| 12(B) | Convert given hexadecimal number 7DF to Base 4 number and base 8 number. | CO 1 | L2 |
| 13(A) | Perform BCD addition i) 1234+4567 ii) 543+187 | CO 1 | L2 |
| 13(B) | 1.Obtain the 2’s complement for the following a)11011010 b) 01110110 2.Obtain the 9’s complement for the following a) 12345678 b) 24681234 | CO 1 | L2 |
| 14(A) | Perform the following operation using 2’s complement form. Assume 8 bit word length including sign bit. (-32) + (-27) | CO 1 | L2 |
| 14(B) | Find the Gray code for the following decimal numbers. i. (73)10 ii. (77)10 | CO 1 | L2 |
| 15(A) | Perform the BCD Subtraction using 10’s Complement for the given Numbers  i) 852 and 253 ii) 325 and 222 | CO 1 | L2 |
| 15(B) | Draw a logic circuit for (A + B)(C + D)C | CO 1 | L2 |
| 16(A) | State and prove DeMorgan’s laws. | CO 1 | L2 |
| 16(B) | Design the circuit diagram for the following Boolean function  **F= ABC’+ DE+ AB’D’** | CO 1 | L2 |
| 17 | Simplify the following Boolean expressions.  1. A’C’+ABC+AC’ to three literals  2. (x’y’+z)’+z+xy+wz to three literals.  3 .(A’+C)(A’+C’)(A+B+C’D) to four literals | CO 3 | L3 |
| 18(A) | Using Boolean laws verify the following equation.  (X+Y’+XY)(X+Y’)X’Y=0 | CO 3 | L3 |
| 18(B) | Using Boolean laws prove that  XY+X’+YZ=X’+Y | CO 3 | L3 |
| 19 | Obtain minimal expression for F = Σ (1, 2, 3, 5, 6, 7, 8, 9, 12, 13, 15) using K – map method. | CO 3 | L3 |
| 20 | Obtain minimal SOP expression using K-Map and hence draw the circuit using 2 input NAND gates  F(A,B,C,D)= | CO 3 | L3 |

**UNIT II**

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| **Q.**  **NO** | **PART A** | **CO** | **LEVEL** |
| 1 | Define Combinational Circuit and sequential circuit. | CO 4 | L1 |
| 2 | Define Half Adder. With a neat sketch draw its logic diagram. | CO 4 | L1 |
| 3 | Define Encoder. Draw its logic diagram and write truth table. | CO 4 | L1 |
| 4 | Differentiate Encoder and Decoder. | CO 4 | L2 |
| 5 | Explain 2X1 Multiplexer. | CO 4 | L1 |
| 6 | Define latch. Draw SR latch using NOR gates. | CO 4 | L1 |
| 7 | Differentiate Latch and Flip flop. | CO 4 | L2 |
| 8 | Define a Register. | CO 4 | L1 |
| 9 | What is the use of Counter? | CO 4 | L1 |
| 10 | Differentiate Synchronous and Asynchronous counter. | CO 4 | L2 |
|  | **PART B** |  |  |
| 11 | Design Full Subtractor using two Half Subtractors with a neat diagram. | CO4 | L3 |
| 12 | Construct the Full Adder with the following steps:  i) Symbolic Representation  ii) Truth Table  iii) Logic Diagram | CO4 | L2 |
| 13 | Discuss in detail about the design procedure for 4 bit binary parallel adder with diagram | CO4 | L2 |
| 14 | Explain about 4X16 decoder. | CO4 | L2 |
| 15 | Explain about priority Encoder with a neat sketch. | CO4 | L2 |
| 16 | Implement the logic function using an 8 X 1 Multiplexer. F (A, B, C, D) = ∑m (1,3,4,11,12,13,14,15) | CO4 | L3 |
| 17 | Explain the SR flip flop with necessary diagrams. | CO4 | L2 |
| 18 | Compare SR flip-flop with JK flip-flop. | CO4 | L4 |
| 19 | Explain about universal Shift register with a neat diagram | CO4 | L2 |
| 20 | Design 4 bit synchronous up counter using T flip-flop. | CO4 | L2 |

**UNIT III**

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| **Q. NO.** | **PART A** | **CO** | **LEVEL** |
| 1 | Define Control Word | CO 2 | L1 |
| 2 | What is a Micro Operation | CO 2 | L1 |
| 3 | List out different operations performed on a stack | CO 2 | L1 |
| 4 | What is Register Address | CO 2 | L1 |
| 5 | Define Program Counter | CO 2 | L1 |
| 6 | What is effective address | CO 2 | L1 |
| 7 | Convert the following expression to Reverse Polish Notation  (3\*4)+(5\*6) | CO 2 | L1 |
| 8 | What is RISC | CO 2 | L1 |
| 9 | How subtraction can be done in 2’s complement | CO 1 | L1 |
| 10 | Draw the hardware for signed magnitude addition and subtraction | CO 1 | L1 |
|  | **PART B** |  |  |
| 11 | Explain about General register Organization | CO2 | L2 |
| 12 | Differentiate the register stack and memory stack | CO2 | L2 |
| 13 | Explain Different types of Instruction Formats | CO2 | L2 |
| 14 | Explain about Reverse Polish Notation with an example | CO2 | L2 |
| 15 | Develop a program to execute Y=(A-B)/(C+D\*E) using one-address, two-address and three-address instructions. | CO2 | L3 |
| 16 | Demonstrate the organization of a 64 - word register stack | CO2 | L2 |
| 17 | Explain the working nature of BCD adder with a neat diagram | CO2 | L1 |
| 18 | What are addressing modes? Explain the various addressing modes with examples. | CO2 | L2 |
| 19 | Explain addition and subtraction with 2’s compliment data | CO2 | L2 |
| 20 | Explain booth multiplication Algorithm with an example | CO2 | L2 |

**UNIT IV**

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| **Q. NO.** | **PART A** | **CO** | **LEVEL** |
| 1 | What is the use of Cache Memory | CO1 | L1 |
| 2 | What is Main memory | CO1 | L1 |
| 3 | Define Multi Programming | CO1 | L1 |
| 4 | Define Bootstrap loader | CO1 | L1 |
| 5 | Define Bidirectional Bus | CO1 | L1 |
| 6 | What is Memory Address Map | CO1 | L1 |
| 7 | What is Content Addressable Memory | CO1 | L1 |
| 8 | Define Match Logic | CO1 | L1 |
| 9 | What is Hit Ratio | CO1 | L1 |
| 10 | What is Address Space and Memory Space | CO1 | L1 |
|  | **PART B** |  |  |
| 11 | Explain about different types of memory hierarchies | CO1 | L2 |
| 12 | Write briefly about auxiliary memory. | CO1 | L1 |
| 13 | What is the reason for not having one large memory unit for storing all information at one place? | CO1 | L1 |
| 14 | Differentiate RAM and ROM | CO1 | L2 |
| 15 | Explain different types of ROM chips | CO1 | L2 |
| 16 | Explain Associative memory in detail | CO1 | L2 |
| 17 | A block set associative cache consists of a total of 64 blocks divided into 4-block sets. The main memory contains 4096 blocks each of 128 words. i. How many bits are there in each of the TAG, SET and WORD fields? ii. How many bits are there in main memory address. | CO1 | L1 |
| 18 | What is cache memory? Also, explain its operation | CO1 | L2 |
| 19 | Analyze the concept of virtual memory with the help of an example. | CO1 | L4 |
| 20 | Explain the following  i) need for cache memory  ii) Locality of reference | CO1 | L2 |

**UNIT V**

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| **Q. NO.** | **PART A** | **CO** | **LEVEL** |
| 1 | Define Control command | CO2 | L1 |
| 2 | What is Asynchronous serial transfer | CO2 | L1 |
| 3 | What is the advantage of start bit and Stop bit in Data transfer | CO2 | L1 |
| 4 | Define programmed I/O | CO2 | L1 |
| 5 | What is the advantage of Input Output Interface | CO2 | L1 |
| 6 | What is the advantage of Status command | CO2 | L1 |
| 7 | What is Interrupt Initiated I/O | CO2 | L1 |
| 8 | Define Priority Interrupt | CO2 | L1 |
| 9 | What is polling | CO2 | L1 |
| 10 | What is interrupt Cycle | CO2 | L1 |
|  | **PART B** |  |  |
| 11 | List out different types of input and output devices | CO2 | L1 |
| 12 | Differentiate I/O bus verses Memory bus | CO2 | L4 |
| 13 | Explain the purpose I/O interfaces between internal storage and external I/O devices. | CO2 | L2 |
| 14 | What is Asynchronous Data Transfer? Explain the operation of Handshaking operation with a neat diagram | CO2 | L2 |
| 15 | Compare strobe control and handshaking. | CO2 | L4 |
| 16 | Differentiate between synchronous and asynchronous data transfer method. | CO2 | L4 |
| 17 | What is DMA? Draw the block diagram of DMA controller? | CO2 | L3 |
| 18 | Explain DMA transfer in a computer system | CO2 | L2 |
| 19 | Demonstrate daisy chaining priority method. | CO2 | L2 |
| 20 | Explain the interrupt cycle execution with the help of neat diagram | CO2 | L2 |

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