DIGITAL LOGIC &COMPUTER ORGANIZATION

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| **Course Code** | **23ES1304** | **Year** | II | **Semester** | I |
| **Course Category** | **Engineering Science** | **Branch** | **CSE** | **Course Type** | PC |
| **Credits** | 3 | **L – T – P** | 3-0-0 | **Prerequisites** | Engineering Mathematics, BEEE |
| **Continuous Evaluation:** | 30 | **Semester**  **End Evaluation:** | 70 | **Total Marks:** | 100 |

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| **Course Outcomes** | | |
| Upon successful completion of the course, the student will be able to: | | |
| **CO1** | Understand the basics of digital circuits, computer system components and organization,  computer arithmetic, and memory organization. | L2 |
| **CO2** | Apply the basic concepts of I/O organization and Processor Organization | L3 |
| **CO3** | Apply the minimization techniques to simplify Boolean expressions | L3 |
| **CO4** | Analyze the functionality of combinational circuits and sequential circuits. | L4 |

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| **Contribution of Course Outcomes towards achievement of Program Outcomes & Strength of**  **correlations (3:Substantial, 2: Moderate, 1:Slight)** | | | | | | | | | | | | | | |
|  | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| **CO1** | 3 |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **CO2** |  |  |  |  |  |  |  |  |  |  |  |  | 2 |  |
| **CO3** | 2 |  |  |  |  |  |  |  |  | 1 |  |  |  |  |
| **CO4** |  | 2 |  |  |  | 3 |  |  | 1 | 1 |  |  |  |  |
| **Avg.** | **2.5** | **2** |  |  |  | **3** |  |  | **1** | **1** |  |  | **2** |  |

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| **Syllabus** | | |
| **Unit**  **No.** | **CONTENTS** | **Mapped**  **CO** |
| **I** | **Data Representation:** Binary Numbers, Number base conversions, Octal and Hexadecimal Numbers, complements of Numbers, Signed binary numbers, Binary codes, Basic Gates  **Digital Logic Circuits-I:** Basic Theorems and Properties of Boolean Algebra, Boolean Functions, Canonical and Standard forms**,** The Map Method, Four-Variable K-map, Product of Sums simplification, Don‟t Care  Conditions | **CO1,CO3** |
| **II** | **Digital Logic Circuits-II**: Combinational Circuits, Analysis of Combinational circuits, Binary Adder – Subtractor, Decoders, Encoders, Multiplexers  **Sequential Circuits** – Latches, Flip-Flops, Shift Registers, Ripple counters,  Synchronous Counters | **CO1,CO4** |

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| **III** | **Processor Organization:** General Register Organization, Stack Organization, Instruction Formats and Addressing Modes  **Computer Arithmetic:** Addition and Subtraction, Multiplication Algorithms, Decimal Arithmetic Unit, Decimal Arithmetic Operations | **CO1,CO2** |
| **IV** | **The Memory Organization:** Memory Hierarchy, Main Memory, Auxiliary Memory, Associative Memory, Cache Memory and Virtual Memory | **CO1** |
| **V** | **Input/output Organization:** Peripheral Devices, Input Output Interface, Asynchronous Data Transfer, Modes of Transfer, Priority Interrupt, DMA | **CO2** |

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| **Learning Resources** |
| **Text Books** |
| 1. Digital Design, 6th Edition, M. Morris Mano, Pearson Education. 2. Computer Systems Architecture, M.Moris Mano, Revised 3rdEdition, Pearson 3. Computer Organization, Carl Hamacher, ZvonkoVranesic, SafwatZaky, 6th edition, McGraw Hill |
| **Reference Books** |
| 1. Computer Organization and Design, David A. Paterson, John L.Hennessy, Elsevier 2. Fundamentals of Logic Design, Roth, 5thEdition, Thomson 3. Computer Organization and Architecture, William Stallings, 11thEdition, Pearson. |
| **E-Resources & other digital material** |
| 1. <https://nptel.ac.in/courses/117105080> 2. <https://archive.nptel.ac.in/courses/106/105/106105163/> 3. <https://nptel.ac.in/courses/106/103/106103068/> |

**Course Coordinators**

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4. Ms P Dedeepya (CSE Dept)

**Prof. & Head, Dept. of CSE Prof. & Head, Dept. of IT**