|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **P.V.P Siddhartha Institute of Technology(Autonomous)** | | | | | | | | | | |
| **Department of Computer Science and Engineering** | | | | | | | | | | |
| **Course:** B.Tech | | | **Year:** II | **Semester:** I | **Descriptive:** II | **A.Y:**2023-24 | | | | |
| **Subject Code:** 20CS3301 | | | **Subject Name:** Fundamentals of Digital Logic Design | | | **Regulation**:PVP20 | | | | |
| **Duration:**  1 hr 30 min | | | **Maximum Marks**:15 Marks | | | **Date**: 29-11-2023 | | | **Session: F.N** | |
| **Answer all the Questions. Each Question carries 5Marks 3×5M=15M** | | | | | | | | | | |
| **Q.No** |  | | | | | | **Marks** | **CO** | | **Level** |
| **1.** | **a)** | Implement Full adder logic using Decoder. | | | | | **2.5** | **CO3** | | **3** |
| **b)** | Design 8\*1 MUX using 4\*1 MUX & 2\*1 MUX | | | | | **2.5** | **CO3** | | **3** |
|  | | | | | | | | | | |
| **2.** | **a)** | Compare SR flip-flop with JK flip-flop. | | | | | **2.5** | **CO4** | | **4** |
| **b)** | Apply the conversion logic to convert D Flip-Flop into T Flip-Flop. | | | | | **2.5** | **CO3** | | **3** |
|  | | | | | | | | | | |
| **3.** | **a)** | Construct the circuit diagram for Four‐Bit Universal Shift Register. | | | | | **2.5** | **CO3** | | **3** |
| **b)** | Design 4 bit synchronous up counter using T flip-flop. | | | | | **2.5** | **CO3** | | **3** |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **P.V.P Siddhartha Institute of Technology(Autonomous)** | | | | | | | | | | |
| **Department of Computer Science and Engineering** | | | | | | | | | | |
| **Course:** B.Tech | | | **Year:** II | **Semester:** I | **Descriptive:** II | **A.Y:**2023-24 | | | | |
| **Subject Code:** 20CS3301 | | | **Subject Name:** Fundamentals of Digital Logic Design | | | **Regulation**:PVP20 | | | | |
| **Duration:**  1 hr 30 min | | | **Maximum Marks**:15 Marks | | | **Date**: 29-11-2023 | | | **Session: F.N** | |
| **Answer all the Questions. Each Question carries 5Marks 3×5M=15M** | | | | | | | | | | |
| **Q.No** |  | | | | | | **Marks** | **CO** | | **Level** |
| **1.** | **a)** | Implement Full adder logic using Decoder. | | | | | **2.5** | **CO3** | | **3** |
| **b)** | Design 8\*1 MUX using 4\*1 MUX & 2\*1 MUX | | | | | **2.5** | **CO3** | | **3** |
|  | | | | | | | | | | |
| **2.** | **a)** | Compare SR flip-flop with JK flip-flop. | | | | | **2.5** | **CO4** | | **4** |
| **b)** | Apply the conversion logic to convert D Flip-Flop into T Flip-Flop. | | | | | **2.5** | **CO3** | | **3** |
|  | | | | | | | | | | |
| **3.** | **a)** | Construct the circuit diagram for Four‐Bit Universal Shift Register. | | | | | **2.5** | **CO3** | | **3** |
| **b)** | Design 4 bit synchronous up counter using T flip-flop. | | | | | **2.5** | **CO3** | | **3** |