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| **P.V.P Siddhartha Institute of Technology(Autonomous)** | | | | | | | | | | | | | | **Signature of Invigilator with date:** | | **Marks Obtained:** | |
| **Department of Computer Science and Engineering** | | | | | | | | | | | | | |
| **Course: B.Tech** | | **Year: II** | | | **Semester: I** | | | | | **Objective: I** | | | |
| **Regulation:PVP20** | | **Maximum Marks:10Marks** | | | | | | | | | | **Session: F.N** | |
| **A.Y:2023-24** | | **Date:27-09-23** | | | | | | | **Duration: 20 min** | | | | |
| **Subject Code:20CS3301** | | | | **Subject Name: Fundamentals of Digital Logic Design** | | | | | | | | | | | | | |
| **Registered Number:** | | | | | | | | | | | **Name:** | | | | | | |
| **Answer all the Questions. Each Question carries ½ Mark 20×½ M=10M** | | | | | | | | | | | | | | | | | |
| **S.No** | **Question** | | | | | | | | | | | | | | **CO** | **Level** | **Answer** |
| 1. | **The representation of hexadecimal number (65F)16 in decimal is** | | | | | | | | | | | | | | **CO1** | **L2** |  |
| a) (1646)10 | | b) (4532)10 | | | | | c) (1631)10 | | | | | d) (5312)10 | |
| 2. | **The octal equivalent of the given binary number 1011101011** | | | | | | | | | | | | | | **CO1** | **L2** |  |
| a) 7353 | | b)1353 | | | | | c) 5651 | | | | | d) 5657 | |
| 3. | **In 16-bit 2’s complement representation, the decimal number -28 is** | | | | | | | | | | | | | | **CO1** | **L2** |  |
| a) 1111 1111 0001 1100 | | b) 0000 0000 1110 0100 | | | | | c)1111 1111 1110 0100 | | | | | d)1000 0000 1110 0100 | |
| 4. | **The 10’s complement of 65347 is** | | | | | | | | | | | | | | **CO1** | **L2** |  |
| a) 45652 | | b) 45655 | | | | | C) 34653 | | | | | d) 45654 | |
| 5. | **Perform addition of BCD numbers: 1000 + 0110** | | | | | | | | | | | | | | **CO1** | **L2** |  |
| a) 0001 0110 | | b) 0001 0100 | | | | | c) 0010 0100 | | | | | d) 0010 0101 | |
| 6. | **Find the complement of the expression (A’+B )( C+D’) is \_\_\_\_\_\_\_\_\_** | | | | | | | | | | | | | | **CO1** | **L2** |  |
| a) AB’+C’D | | b) (A + B’)(C’ + D) | | | | | c) A’B+CD’ | | | | | d)(A+B)(C+D) | |
| 7. | **If we add an inverter at the output of AND gate, what function is produced?** | | | | | | | | | | | | | | **CO1** | **L2** |  |
| a) NOR | | | | | | | b) Ex-NOR | | | | | | |
| c) NAND | | | | | | | d) Ex-OR | | | | | | |
| 8. | **In Boolean algebra,(A.A’)+A=?** | | | | | | | | | | | | | | **CO1** | **L2** |  |
| a)A | | b) 0 | | | | | c)A’ | | | | | d) 1 | |
| 9. | **Which of the following options correctly represents the consensus law of digital circuits?** | | | | | | | | | | | | | | **CO1** | **L2** |  |
| a) AB+A’C+BC=AB+A’C | | | | | | b) A’B+A’C+BC=AB+A’C | | | | | | | |
| c) AB+A’C+BC=AB+A’C’ | | | | | | d) A’B+A’C+BC=AB+A’C’ | | | | | | | |
| 10. | **There are \_\_\_\_\_\_\_\_\_\_\_\_\_ Minterms for 3 variables (a, b, c).** | | | | | | | | | | | | | | **CO1** | **L2** |  |
| * a) 4 | | * b) 6 | | | | | * c) 8 | | | | | * d)16 | |
| 11. | **How many NAND gates are required to implement OR gate** | | | | | | | | | | | | | | **CO1** | **L2** |  |
| a) 1 | | b) 2 | | | | | c) 3 | | | | | d) 4 | |
| 12. | **X+XY =X represent which law?** | | | | | | | | | | | | | | **CO1** | **L2** |  |
| a) Commutative | | b) Absorption | | | | | c) Distributive | | | | | d) Idempotent | |
| 13. | **In K-map a “octet” is group of \_\_\_\_\_\_\_\_\_\_1’s** | | | | | | | | | | | | | | **CO1** | **L2** |  |
| a) 4 | | b) 8 | | | | | c) 2 | | | | | d) 16 | |
| 14. | **How many OR gates are required to realize Y = AB’ + CF + D?** | | | | | | | | | | | | | | **CO1** | **L2** |  |
| 1. 4 | | | | | | | 1. 5 | | | | | | |
| 1. 3 | | | | | | | 1. 2 | | | | | | |
| 15. | **The Logic expression F = AB’C+ ABC +A’BC’ is in** | | | | | | | | | | | | | | **CO1** | **L2** |  |
| a) standard SOP form | | | | | b) canonical POS form | | | | | | | | |
| c) canonical SOP form | | | | | d) standard POS form | | | | | | | | |
| 16. | **Simplify F(x, y, z) =∑ (0, 2,3,5,6, 7) ------------------------------** | | | | | | | | | | | | | | **CO1** | **L2** |  |
| 17. | **The output expression for SUM and CARRY of a half adder are \_\_\_\_\_\_\_\_\_\_** | | | | | | | | | | | | | | **CO1** | **L2** |  |
| 1. S= A EX-NOR B   C=A’B | | b) S= A EX-OR B  C=AB | | | | | c) S= A OR B  C=AB | | | | | 1. S= A and B   C=AB’ | |
| 18. | **Which of the following is a type of digital logic circuit?** | | | | | | | | | | | | | | **CO1** | **L2** |  |
| 1. Combinational logic Circuits | | 1. Sequential logic Circuits | | | | | c) Both | | | | | d) None | |
| 19. | **In combinational circuit the output depends only on \_\_\_\_\_ inputs** | | | | | | | | | | | | | | **CO1** | **L2** |  |
| a) Future | | b) Past | | | | | c)Present and past | | | | | d) Present | |
| 20. | **Which of the following logic circuits accepts three binary digits on inputs, and produces two binary digits, a sum bit and a carry bit on its outputs?** | | | | | | | | | | | | | | **CO1** | **L2** |  |
| a) Half Adder | | b) Full Adder | | | | | c)Serial Adder | | | | | d) Parallel Adder | |