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| **P.V.P Siddhartha Institute of Technology(Autonomous)** |
| **Department of Computer Science and Engineering** |
| **Course: B.Tech** | **Year: II** | **Semester: I** | **Descriptive: I** | **A.Y:2023-24** |
| **Subject Code: 20CS3301** | **Subject Name: Fundamentals of Digital Logic Design** | **Regulation:PVP20** |
| **Duration:****1 hr 30 min** | **Maximum Marks:15 Marks** | **Date:27-09-23** | **Session: F.N** |
| **Answer all the Questions. Each Question carries 5Marks 3×5M=15M** |
| **Q.No** |  | **Marks** | **CO** | **Level** |
| **1.** | **a)** | Translate the following base conversions.i) (4021.2)5 = ( )10 ii) (153)10 = ( )16iii) (DB4F)16 = ( )2 =( )8 | **3** | **CO1** | **2** |
| **b)** | i) Show the subtraction operation using 10’s complement 72532– 3250ii)Build logic circuit for the given Boolean expression F=[(A+B)C]’+BD’ | **2** | **CO1** | **2** |
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| **2.** | **a)** | Apply the Boolean laws to simplify the following expressions:i) F = C + AB + AD(B + C )+ CDii) F = xy+x(wz+wz’) | **3** | **CO2** | **3** |
| **b)** | Apply K-Map method to simplify the following Boolean function:i) F(A, B, C, D) =∑m(0,4,8,10,12,13,15) +d(1,2)ii) F(A,B,C,D) = π(1,2,3,8,9,11,14)  | **2** | **CO2** | **3** |
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| **3.** | **a)** | Build a logic Diagram for the Half Adder with a neat sketch. | **2** | **CO3** | **3** |
| **b)** | Construct the Full Adder with the following steps:1. Block diagram
2. Truth Table and output expressions
3. Logic Diagram
 | **3** | **CO3** | **3** |