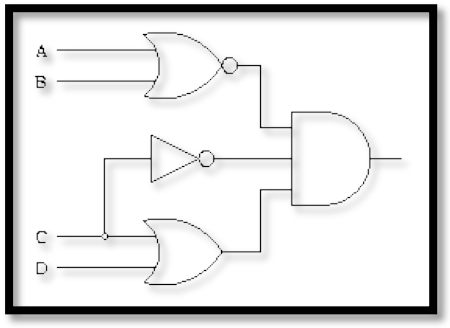
P.V.P SIDDHARTHA INSTITUTE OF TECHNOLOGY		
BRANCH : Computer Science and Engineering		**REGULATION : PVP20**
Course: B. Tech	**SUBJECT : Fundamentals of Digital Logic Design**	
Subject Code: 20CS3301/20IT3301		**Year and Semester: II Year / I Sem**
QUESTION BANK		

UNIT I

Q. NO	QUESTION	CO	LEVEL
1(A)	Explain the Characteristics of Digital System.	1	L2
1(B)	Explain the difference between analog and digital systems.	1	L2
2(A)	Convert the following numbers i)$(163.789)_{10}$ to Octal number ii)$(11001101.0101)_2$ to base-8 and base-4 iii)$(4567)_{10}$ to base2 iv) $(4D.56)_{16}$ to Binary	1	L2
2(B)	Subtract $(111001)_2$ from $(101011)_2$ using 1's complement?	1	L2
3	Convert the following numbers i) $(615)_{10}$ = ( )$_{16}$ ii)) $(214)_{10}$ = ( )$_8$ iii)$(0.8125)_{10}$=( )$_2$ iv) $(658.825)_{10}$=( )$_8$ v)$(54)_{10}$=( )$_2$	1	L2
4(A)	i) Perform (28)+(-15) in binary using signed binary numbers ii) Perform (-50)-(-10) in binary using the signed-2's complement	1	L2
4(B)	Convert the decimal number 3452 in i)BCD ii)Excess-3	1	L2
5(A)	Convert the following numbers i) $(250.5)_{10}$ = ( )$_2$ ii)) $(673.23)_{10}$ = ( )$_8$ iii)$(101110.01)_2$=( )$_8$	1	L2
5(B)	Convert the following number $(AB33)_{16}$ to Binary and Gray code	1	L2
6(A)	Perform the following $(7129)_{10}$ + $(7711)_{10}$ using BCD arithmetic	1	L2
6(B)	Explain the use of complements? Perform the subtraction using 9's complement for the given Base-9 numbers (565)-(666).	1	L2
7	Explain the Binary Codes with examples	1	L2
8(A)	Perform the BCD Addition for the given Numbers i) 984 and 599 ii) 429 and 476	1	L2
8(B)	Perform the BCD Subtraction using 10's Complement for the given Numbers i) 852 and 253 ii) 325 and 222	1	L2
9(A)	Convert the Hexa decimal number to Octal and vice versa with an example.	1	L2
9(B)	Explain the Excess-3 code? Convert given Excess-3 code (01011100) to Binary Code.	1	L2
10(A)	Convert the given numbers Gray Code to Binary Code i) 1011 ii) 110101 iii) 10110	1	L2
10(B)	Perform the BCD Subtraction using 9's Complement i) $(35)_{10}$ and $48_{(10)}$	1	L2
10(C)	Explain the Self-Complement Code? Solve $(356)_{10}$ are Self-Complement.	1	L2

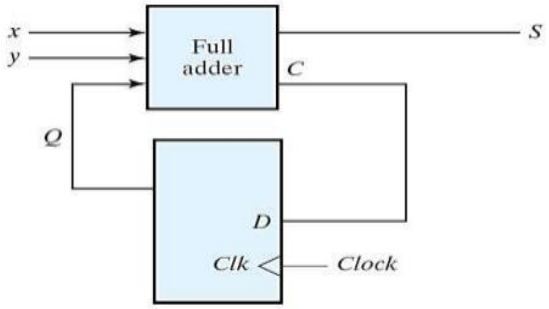
UNIT II

Q. NO	QUESTION	CO	LEVEL
1	Simplify the Boolean expressions to minimum number of literals i) (A + B)(A + C')(B' + C') ii) AB + (AC)' + AB'C (AB + C) iii) (A+B)' (A'+B')'	2	L3
2(A)	Obtain the Complement of Boolean Expression i) A+B+A'B'C ii) AB + A (B +C) + B'(B+D)	2	L3
2(B)	Design the circuit diagram for the following Boolean function **F= ABC'+ DE+ AB'D'** using NAND gates.	2	L3
3	Obtain the a) SOP b) POS expression for the function given below **F(A,B,C,D)= = Σm(0,1,2,5,8,9,10)**	2	L3
4	Explain Postulates and theorems of Boolean Algebra.	2	L2
5(A)	Construct truth table of the function: i) F = xy+ xy'+ y'z ii) F = bc+ a'c'	2	L3
5(B)	Simplify the following Boolean expressions to a minimum number of literals and draw the logic diagrams (i) xy+ xy' (ii) (x + y) (x + y') (iii) xyz + x'y+ xyz'	2	L3
6	State and Explain the DeMorgan's Theorem and Consensus Theorem with examples.	2	L3
7	Minimize the SOP and POS forms of the following Boolean function using K-map and draw the corresponding logic diagrams: **F(A,B,C) = ∑ m(0,2,8,9,10,15) + d(1,3,6,7)**	2	L3
8(A)	Draw a logic circuit for (A + B)(C + D)C	2	L3
8(B)	Find the output in the Digital Logic Circuit. 	2	L3
9	Minimize the following expressions using K-map: a) f(w,x,y,z) = Σm(4,5,7,12,14,15) +d(3,8,10) b) F(A,B,C,D) = ∑m(1,3,7,11,15) + ∑d(0,2,5)	2	L3
10	Simplify the Boolean expression using K-map and implement using NAND gates : **F(A,B,C,D) = Σm(0,2,3,8,10,11,12,14)**	2	L3

UNIT III

Q. NO.	QUESTION	CO	LEVEL
1	a) Identify the steps involved in design procedure of combinational circuits b) Difference between Decoder and Encoder c) Define Priority Encoder with example.	**3**	**L3**
2	What is decoder? Construct a 4X16 decoder with two 3X8 decoders**.**	**3**	**L3**
3	Design and draw a Full Subtractor using two Half Subtractor.	**3**	**L3**
4	Design a 4 bit parallel adder using Full adder.	**3**	**L3**
5	Design an 8-bit BCD adder using 4-bit binary adder.	**3**	**L3**
6	Implement the full adder using two 4X1 multiplexers.	**3**	**L3**
7(A)	Implement the 8X1 multiplexer for the following Boolean function **F(A,B,C.D) = Σm (0,1,2,5,7,8,9,14,15)**	**3**	**L3**
7(B)	Explain multiplexer and its applications.	**1**	**L2**
8(A)	Obtain the functions for the combinational circuit in sum-of-minterms to form Decoders. **F1= X'Y'Z' + XZ** **F2 = XY'Z' + X'Y** **F3= X'Y'Z' + XY**	**3**	**L3**
8(B)	Implement 4 line to 16 line decoder for the following Boolean function. **F1= Σm (0, 1, 4, 7, 12, 14, 15)** **F2= Σm (1, 3, 6, 9, 12)** **F3= Σm (2, 3, 7, 8, 10)** **F4= Σm (1, 3, 5)**	**3**	**L3**
9	Construct 4X1 multiplexer using logic gates.	**3**	**L3**
10	Obtain the function f(A,B,C,D) = Σ(1,2,3,4,6,7,8,10,12,14,15) and design a i) 8X1 MUX ii) 4X1 MUX	**3**	**L3**

UNIT IV

Q. NO.	QUESTION	CO	LEVEL
1(A)	Compare combinational and sequential circuits.	**4**	**L4**
1(B)	Distinguish between the Latch and Flip.	**4**	**L4**
2	Construct SR Latch and D Latch with Truth Table and Logic Diagram.	**3**	**L3**
3	Explain the following with Truth Table ,characteristic equation and Excitation table i) J-K flip-flop ii) S- R flip-flop iii) D flip-flop	**1**	**L2**
4	Construct the D and T flip flop with logic diagrams and function table.	**3**	**L3**
5	Compare SR Flip Flop and JK Flip Flop.	**4**	**L4**
6	Design the conversion logic to convert JK Flip-Flop into T- Flip-Flop. **(**	**3**	**L3**
7	Design the conversion logic to convert SR Flip-Flop into JK Flip-Flop.	**3**	**L3**
8	Explain the Master-Slave J-K flip-flop?	**1**	**L2**
9	Derive the characteristic equation of JK flip-flop from Excitation table.	**3**	**L3**
10	A sequential circuit consists of a full-adder circuit connected to a D flip-flop, as shown in given figure .Design the state table and state diagram of the sequential circuit. 	**3**	**L3**

UNIT V

Q. NO.	QUESTION	CO	LEVEL
1	Design a BCD ripple counter using JK flip-flop.	3	L3
2	Compare ripple counter and synchronous counter.	4	L4
3	Design a 4-bit ripple counter and draw the timing diagram of that counter.	3	L3
4	Design a four-bit binary synchronous counter with D flip-flop.	3	L3
5	List the application of shift register? Explain in detail.	4	L4
6	Design the 4- bit register with parallel load.	3	L3
7	Construct the circuit diagram for Four - bit universal shift register.	3	L3
8	Explain truth table and circuit diagram of serial adder.	2	L2
9	Implement the logic circuit diagram for Four - bit Binary Ripple Counter.	3	L3
10	Design Up Down Binary Counter with Logic Diagram.	3	L3

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