Code No: 20CS3301/20IT3301

PVP SIDDHARTHA INSTITUTE OF TECHNOLOGY

(Autonomous)

20CS3301/20IT3301-Fundamentals of Digital Logic Design (Common to CSE, IT)

Duration: 3 Hours Max. Marks: 70

Note:

- 1. This question paper contains 5 essay questions with an internal choice.
- 2. Each question carries 14 Marks.
- 3. All parts of Question paper must be answered in one place

 $5 \times 14 = 70 \text{ Marks}$

			Blooms Level	СО	Max. Marks			
UNIT-I								
1	(a)	Convert the following base conversions using Number System i. $(53.625)_{10}$ to $(?)_2$ ii. $(3FD)_{16}$ to $(?)_2$ iii. $(A69.8)_{16}$ to $(?)_{10}$	L2	CO1	7M			
	(b)	Perform the decimal subtraction in 8-4-2-1 BCD using 9's complement. i) Subtract 79 from 26 ii) Subtract 748 from 983.	L2	CO1	7M			
		OR	•					
2	(a)	Show the Gray code for the following decimal numbers. i) 37 ₁₀ ii) 97 ₁₀ .	L2	CO1	7M			
	(b)	Explain the various logic gates and give the representation along with the truth tables.	L2	CO1	7M			
	•	UNIT-II	•	•				
3	(a)	Obtain the simplified expression in SOP form of $F(a, b, c, d, e) = \sum (1,2,4,7,12,14,15,24,27,29,30,31)$ using K-maps.	L3	CO2	7M			
	(b)	Simplify the following Boolean functions, using a four variable Karnaugh map method and implement the simplified function using NAND gates $F(A,B,C,D) = \sum 0.2.4.5.6.7.8.10.13.15$	L3	CO2	7M			
OR								
4	(a)	Obtain the simplified expression in product of sums) using K-maps i) $F(A,B,C,D) = \pi(0,1,2,3,4,10,11)$ ii) $F(A,B,C,D) = \pi(1,3,5,7,13,15)$	L3	CO2	7M			
	(b)	With the use of K-Map method to simplify the following Boolean expression. $F(w, x, y, z) = \Sigma(2, 3, 5, 6, 11, 14, 15)$	L3	CO2	7M			

(a) Construct the truth table of 3 bit gray to binary code conversion. Show the realization using 4X1 MUX? (b) Design a full binary adder with the use of two half adders and a OR gate. OR (a) Design an 8-bit BCD adder using 4-bit binary adder. (b) Implement the full adder using two 4:1 multiplexers. UNIT-IV (a) Design the conversion logic to convert SR Flip-Flop into JK Flip-Flop. (b) Compare combinational and sequential circuits. Construct the D and T flip flop with logic diagrams and function table. (a) Construct the D and T flip flop and JK Flip-Flop. (b) Distinguish between the SR Flip Flop and JK Flip-Flop. UNIT-V (a) Design a BCD ripple counter using JK flip-flop. (b) Design a three bit counter that counts up when a control variable E = 1. OR (a) Design a 4-bit ripple counter and draw the timing diagram of that counter. (b) Design a four-bit binary synchronous counter with D flip-flops L3 CO3 7M L3 CO3 7M L4 CO4 7M CO3 7M L5 CO3 7M			UNIT-III							
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Cost	0	(b)	Implement the full adder using two 4:1 multiplexers.	L3	CO3	7M				
The flop is the property of	UNIT-IV									
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10 (a) counter. L3 CO3 7M		OR								
(b) Design a four-bit binary synchronous counter with D flip-flops L3 CO3 7M	10	(a)		L3	CO3	7M				
		(b)	Design a four-bit binary synchronous counter with D flip-flops	L3	CO3	7M				

Course Coordinators

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