**Prasad V Potluri Siddhartha Institute OF TECHNOLOGY(Autonomous)**

**DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING**

**REGULATION-PVP20**

**Computer orGanization & Architecture**

**II B.Tech - I Semester**

**QUESTION BANK**

**UNIT-1**

1) Construct a bus system using four registers with 4-bit each using multiplexers (CO2-L3)

2) Construct a 4-bit binary Adder – Subtractor (CO2-L3)

3) Construct a digital circuit that performs the four logic operations of exclusive OR, exclusive-NOR, NOR, and NAND. Use two selection variables. Show the logic diagram of one typical stage. (CO2-L3)

4) Design an Arithmetic Logic Shift unit. (CO2-L3)

5) Design a 4-bit arithmetic circuit using four full adders. (CO2-L3)

6) Construction of bus system for 8 registers with 16 bits each (CO2-L3)

 No of multiplexers=?? Size of each multiplexer=??? Bus selection ????????

7) Build a digital circuit that performs arithmetic micro operations(CO2-L3)

8) Make use of logic micro operations to manipulate bits of a register(CO2-L3)

9) With a neat sketch, explain 4-bit combinational circuit shifter. (CO2-L3)

**UNIT-2**

1) Explain about instruction codes with an example. (CO2-L2)

2) Construct a flow chart for instruction cycle. (CO2-L3)

3) Explain in detail memory reference instructions. (CO1,CO2-L2)

4) Discuss about Program Interrupt(CO2-L2)

5) Construct a flowchart to handle interrupts during execution. (CO2-L3)

6) Differences between Direct and Indirect Addressing of Memory? (CO2-L3)

7) Differences between Hardwired and Micro programmed Control? (CO2-L3)

8) Explain the three different types of instruction formats used in basic computer(CO2-L2)

9) Demonstrate the usage of interrupt cycle during the execution of Input / Output instruction(CO2-L3)

10) What is instruction set completeness? (CO2-L1)

**UNIT-3**

1) Make use of stack organization to evaluate these expressions. If D=2, X=3,Y=4, Z=5 (CO3-L3)

 a. X+Y+Z b. X\*(Y+Z) c. X\*Y+Z\*D

2) Convert the following expressions into reverse polish notation(CO3-L3)

a. X+Y+Z b. X\*(Y+Z) c. A+B/C\*(D+E\*F)

3) Explain the process of selection of General register organization? (CO1,CO3-L2)

4) Develop a program to implement X= (A\*B)+(C+D)/ E using the following Instruction Formats. (CO3-L3)

1. Using a general register computer with three address instructions.
2. Using a general register computer with two address instructions.
3. Using an accumulator type computer with one address instructions.

Using a stack organized computer with zero-address operation instructions.

5) Utilize the following memory values and a one-address machine with an accumulator, what values do the following instructions load into accumulator? (CO3-L3)

• Word 20 contains 40

• Word 30 contains 50

• Word 40 contains 60

• Word 50 contains 70

Instructions are-

1. Load immediate 20

2. Load direct 20

3. Load indirect 20

4. Load immediate 30

5. Load direct 30

6. Load indirect 30

6) Illustrate various data transfer, manipulation and program control instructions with examples. (CO3-L2)

7) What are the three types of CPU organizations and explain with an example? (CO1,CO3-L2)

8) Discuss logical and bit manipulation instructions. (CO3-L2)

9) Evaluate the arithmetic statement X = (A + B) \* (C + D) using zero, one, two and three address instructions. (CO3-L3)

10) Discuss in detail about Addressing modes with suitable Examples? (CO3-L2)

**UNIT-4**

1) Explain about an associative memory page table (CO4-L2)

2) What is memory hierarchy? Explain with a block diagram. What is the reason for not having one large memory unit for storing all information at one place? (CO4-L2)

3) A digital computer has a memory unit of 64K + 16 and a cache memory of 1K words. Cache uses direct mapping with a block size of 4 words. (CO4-L3)

 i) How many bits are there in the tag, index, block and word fields of the address format?

 ii) How many bits are there in each word of cache, and how are they divided into functions? Include a valid bit.

iii) How many blocks can the cache accommodate?

 4) Perform the arithmetic operations below with binary numbers and with negative numbers in signed-2"s complement representation. Use seven bits to accommodate each number together with its sign. In each case, determine if there is an overflow by checking the carries Into and out of the sign bit position . (CO2-L2)

a) (+35) + (+40)

 b) (-35) + (-40)

c) (-35) - (+40)

 5) Show the step-by-step multiplication process using Booth algorithm for the binary numbers (+15) X (-13) (CO2-L3)

 6) Construct a flow chart for Addition and Subtraction of two signed magnitude numbers (CO2-L3)

 7) Distinguish between various cache mapping techniques. (CO4-L4)

 8) Analyze the concept of Virtual memory. (CO4-L4)

 **UNIT-5**

1) Compare I/O vs memory bus and explain functions of IO Interface circuit with a neat sketch. (CO4-L4)

2) Distinguish strobe and handshaking asynchronous data transfer methodologies. (CO4-L4)

3) Classify the parallel processing models using Flynn’s Classification. (CO4-L4)

4) Analyze Arithmetic Pipeline concept using floating point Addition and Subtraction. (CO4-L4)

5) What is DMA? Draw the block diagram of DMA controller? (CO4-L2)

6) What is meant by pipelining? Why do we require instruction pipelining? (CO4-L2)

7) Determine the number of clock cycles that it takes to process 200 tasks in a six-segment pipeline. (CO4-L3)

8) Explain Daisy chaining priority interrupt. (CO4-L2)