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| **20CS3303** | | | | |  | |  | | | |
|  | | | | | **Computer Organization and Architecture** | | | | | |
|  | | | | | | | | | | |
| **Offering Branches:** | | | | CSE | |  | |  | | |
| **Course Category:** | | | | Program Core | | **Credits:** | | 3 | | |
| **Course Type** | | | | Theory | | **Lecture-Tutorial- Practical:** | | 3-0-0 | | |
| **Prerequisites:** | | | | Foundations of Digital Logic Design | | **Continuous Evaluation:** | | 30 | | |
| **Semester End Evaluation:** | | 70 | | |
| **Total Marks:** | | 100 | | |
| **Course Outcomes** | | | | | | | | | | |
| Upon successful completion of the course, the student will be able to: | | | | | | | | | | |
| **CO1** | | Understand the basic functional units of a computer system and its organization. | | | | | | | | **L2** |
| **CO2** | | Apply appropriate instructions for processing various types of computer operations | | | | | | | | **L3** |
| **CO3** | | Applying various types of organizations on registers and make an effective report | | | | | | | | **L3** |
| **CO4** | | Analyze memory hierarchy, I/O communication and pipelining | | | | | | | | **L4** |
| **Course Content** | | | | | | | | | | |
|  | | | | | | | | | | |
| **UNIT-1** | | | **Register Transfer and Micro Operations:**  Register Transfer Language, Register Transfer, memory Transfers, Bus construction with Multiplexers, Arithmetic Micro operations, Logic Micro Operations, Shift Micro-operations, Arithmetic Logic Shift Unit. | | | | | | CO1,CO2 | |
| **UNIT-2** | | | **Basic Computer Organization:**  Instruction codes, Computer Registers, Computer Instructions, Timing and Control, Instruction Cycle, Memory-Reference Instructions, Input-Output and Interrupt. | | | | | | CO1,CO2 | |
| **UNIT-3** | | | **Central Processing Unit:**  General registers Organization, Stack Organization, Instruction Formats, Addressing Modes, Data Transfer and Manipulation, Program Control. | | | | | | CO1, CO3 | |
| **UNIT-4** | | | **Computer Arithmetic:**  Introduction, Addition and Subtraction, Booth Multiplication Algorithm.  **Memory Organization**: Memory Hierarchy, Main Memory, Auxiliary memory, Associative Memory, Cache Memory, Virtual Memory | | | | | | CO1, CO2,CO4 | |
| **UNIT-5** | | | **Input-Output Organization:** Peripheral Devices, Input output Interface, Asynchronous Data Transfer, Priority Interrupt, Direct Memory Access (DMA), Input-Output Processor.  **Pipeline and Parallel Processing**: Parallel processing, Pipelining, Arithmetic pipeline, Instruction pipeline. | | | | | | CO1,CO4 | |
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| **LearningResources** | | | | | | | | | | |
| Text book: | | | | | | | | | | |
| 1 | Computer System Architecture, Morris M.Mano, Third Edition,1992,Pearson. | | | | | | | | | |
| References : | | | | | | | | | | |
| 1 | Computer Organization and Architecture,WilliamStallings,EighthEdition,2010,PHI | | | | | | | | | |
| 2 | Computer Organization,CarlHamachar,Vranesic,2002,McGrawHill | | | | | | | | | |
| e-Resources and other Digital Material: | | | | | | | | | | |
| 1 | https://nptel.ac.in/courses/106/106/106106092/ | | | | | | | | | |